PA 1085035

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

October 27, 2003

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: *60/427,197*
FILING DATE: *November 18, 2002*

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS

W. Montgomery

W. MONTGOMERY
Certifying Officer

11-19-02 60427197 APPROV

PTO/SB/16 (10-01)
Approved for use through10/31/2002 OMB 0651-0032
U S Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. ET 656539693US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Charles J.	Razzell	Pleasanton, California

☐ Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max)

AUTOMATIC GAIN CONTROL USING SIGNAL AND INTERFERENCE POWER TO OBTAIN EXTENDED BLOCKING PERFORMANCE

CORRESPONDENCE ADDRESS

Direct all correspondence to:

☐ Customer Number _____ → Type Customer Number here

OR

☐ Firm or Individual Name

Address

Address

City | State | ZIP

Country | Telephone | Fax

24738
PATENT TRADEMARK OFFICE

ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification Number of Pages 18

☒ Drawing(s) Number of Sheets 6

☐ Application Data Sheet. See 37 CFR 1.76

☐ CD(s), Number

☐ Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant claims small entity status. See 37 CFR 1.27.

☒ A check or money order is enclosed to cover the filing fees

☐ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number: _____

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE AMOUNT ($): 160.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government

☒ No

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE Raymond J. Werner

Date 11/18/2002

TYPED or PRINTED NAME Raymond J. Werner

REGISTRATION NO. (if appropriate) 34,752

TELEPHONE 503.466.2294

Docket Number: US020453P

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Washington, D.C. 20231.

FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 160.00

Complete if Known

Application Number	N/A
Filing Date	18 NOV 2002
First Named Inventor	Charles J. Razzell
Examiner Name	N/A
Group Art Unit	N/A
Attorney Docket No.	US020453 P

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☒ Money Order ☐ Other ☐ None

☐ Deposit Account.

Deposit Account Number:

Deposit Account Name:

The Commissioner is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments

☐ Charge any additional fee(s) during the pendency of this application

☐ Charge fee(s) indicated below, except for the filing fee

to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	160.00

SUBTOTAL (1) ($) 160.00

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

			Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X		=	
Independent Claims		-3** =		X		=	
Multiple Dependent						=	

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) ———

**or number previously paid, if greater, For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1 129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) ____________

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) ———

SUBMITTED BY

				Complete (if applicable)	
Name (Print/Type)	Raymond J. Werner	Registration No. (Attorney/Agent)	34,752	Telephone	503.466.2294
Signature	Raymond J. Werner			Date	18 NOV 2002

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

PATENT

PROVISIONAL APPLICATION FOR

AUTOMATIC GAIN CONTROL USING SIGNAL AND INTERFERENCE POWER TO OBTAIN EXTENDED BLOCKING PERFORMANCE

Inventor: Charles J. Razzell

"Express Mail" mailing label number ET 656539693 US

[redacted]

AUTOMATIC GAIN CONTROL USING SIGNAL AND INTERFERENCE POWER TO OBTAIN EXTENDED BLOCKING PERFORMANCE

Background of the Invention

Field of the Invention

The present invention relates generally to automatic gain control circuitry, and more particularly relates to radio receivers that have channel selectivity functions implemented, at least partly, in the digital domain, and which employ one or more analog-to-digital converters in the signal path.

Background

Traditional radio receiver design implemented the required selectivity functions in the analog domain. Such analog filtering has been in use in radio receivers for many years. More recently, digital signal processing techniques, sometimes referred to as digital filtering, have been developed which are well-suited for implementing various functions in radio receivers which, in the past, were exclusively implemented in the analog domain. However, it will be appreciated that in order to utilize the advantages of digital signal processing, analog signals are converted to digital signals prior to being presented for digital signal processing. It will be further appreciated that a common term for a circuit or system used to convert analog signals to digital signals is analog-to-digital converter (ADC).

Various receiver architectures make use of a combination of analog and digital signal processing. Referring to Fig. 1, a conventional radio receiver architecture which makes use of digital selectivity is shown. In this example of a direct conversion radio receiver, the I and Q (i.e., in-phase and quadrature) signals are converted to a digital format, and subsequent digital signal processing, or filtering, is applied to complete the channel filter response. This is in contrast to older architectures wherein most, it not all, selectivity was performed in the analog domain. These older architectures thus provided excellent protection for the A/D converters because large out-of-band signals had already been filtered out in the

analog domain. In this way, out-of-band signal energy was prevented from contributing to the signal amplitude that was presented to the A/D converters.

What is needed are methods and apparatus for reducing or eliminating the signals which exceed the maximum acceptable input level of an analog-to-digital converter in a radio receiver which implements selectivity in the digital domain.

Summary of the Invention

Briefly, embodiments of the present invention provide for improved operation of radio receivers that include analog and digital signal processing portions, with at least one analog-to-digital (A/D) converter disposed between the analog and digital signal processing portions, and wherein the selectivity function of the receiver is, at least partly, implemented in the digital domain. An AGC controller sets a first variable gain amplifier to a low gain state upon a determination that a wide-band signal energy estimation exceeds a wide-band threshold. Such a wide-band threshold is selected so as to reduce, or prevent, the occurrence of saturation of the at least one A/D converter. If the wide-band signal energy estimation is less than the wide-band threshold, then for each of the variable gain amplifiers in the analog portion of the receive signal path, a determination is made as to whether a narrow-band signal energy estimate exceeds a narrow-band threshold, corresponding to that variable gain amplifier, plus a hysteresis value, in which case that variable gain amplifier is set to a low gain state; or whether the narrow-band signal energy estimate is less than the narrow-band threshold minus a hysteresis value, in which case that variable gain amplifier is set to a high gain state.

Brief Description of the Drawings

Fig. 1 is a schematic block diagram of radio receiver having both analog and digital portions, and employing digital selectivity.

Fig. 2 is frequency versus magnitude diagram of an analog transfer function showing wide-band susceptibility.

Fig. 3 is a schematic block diagram of radio receiver having both analog and digital portions, employing digital selectivity, and more specifically illustrating automatic gain control derived only from on-channel (i.e., in-band) signal energy.

Fig. 4 is a schematic block diagram of a digital portion of a radio receiver showing the additional signal paths used to a achieve a wide-band power estimate in accordance with the present invention.

Fig. 5 is a C language segment illustrating an AGC algorithm in accordance with the present invention.

Fig. 6 is a high-level schematic block diagram of one channel of a decimation and filtering scheme, and illustrating access to wide-band signals used for power estimation in accordance with the present invention.

Detailed Description

Methods and apparatus for preventing, or reducing, the occurrence of saturating an A/D converter, which is disposed between an analog portion and a digital portion of a radio receiver, provide for control of one or more variable gain amplifiers based on the total signal energy reaching the A/D converters of the receiver.

Reference herein to "one embodiment", "an embodiment", or similar formulations, means that a particular feature, structure, operation, or characteristic described in connection with the embodiment, is included in at least one embodiment of the present invention. Thus, the appearances of such phrases or formulations herein are not necessarily all referring to the same embodiment. Furthermore, various particular features, structures, operations, or characteristics may be combined in any suitable manner in one or more embodiments.

Terminology

A/D refers to analog-to-digital, as is often used in the context of referring to an A/D converter (ADC).

The acronym AGC refers to automatic gain control.

The acronym ALC refers to automatic level control.

The acronym CDMA refers to code division multiple access.

The acronym ERP refers to effective radiated power.

The acronym PCS refers to personal communication services.

The acronym RSSI refers to received signal strength indicator.

The expression, direct conversion receiver, refers to a radio that converts an incoming signal from a first frequency to a second, desired, frequency in one mixing operation, i.e., without any intermediate frequency (IF) stages.

The present invention relates to radio receivers that have their channel selectivity at least partly implemented in the digital domain, and employ one or more A/D converters in the signal path. In one aspect of the present invention, the total signal power, including out-of-band power, arriving at the input of the A/D converters is maintained within a safe working limit. Such a safe working limit ensures that the signal path is not blocked by strong interferers. In a second aspect of the present invention, digital automatic level control of the fully filtered, on-channel signal provides improved representation of the signal in a given limited word size. Various embodiments of the present invention, which incorporate the aspects mentioned above, are able to provide control of the amplitude of the wanted signal to within well-defined limits. It is noted that the wanted signal is the metric typically used for describing, comparing, or evaluating automatic gain control in an analog portion of a radio receiver.

Conventionally, AGC systems (or subsystems or circuits) are designed to control the level of a desired signal, after channel selectivity has been accomplished. It is therefore a conventional design goal to minimize the impact of off-channel signals on the AGC control loop. It is possible to reproduce this behavior in digital receivers by deriving the AGC power level detection from the output of the final stage of the digital filtering, that is, in the digital baseband. However, enough headroom

has to be left "vacant" in the A/D converters to allow the weakly filtered and/or powerful interferers to be handled linearly.

When no attempt is made to control out-of-band power, this power may exceed the linear range of the A/D converters with undesirable consequences for the signal path. Such undesirable consequences may include the catastrophic consequence of all communication being suddenly lost. Embodiments of the present invention overcome this deficiency by ensuring that the total incident power at the A/D converters does not exceed the linear signal handling range of those A/D converters, even if that means sacrificing some signal-to-noise ratio for the wanted signal.

In an illustrative embodiment of the present invention, the wideband power of the signal at the input to the A/D converters is estimated, and this information is made available as a signal, which is referred to herein as a power signal. For those types of A/D converters that sample directly at the required resolution and sample rate, such a signal may be provided by taking the sums of the squares of digital samples from an in-phase channel and a quadrature channel, and low-pass filtering those sums. In the case of sigma delta A/D converters, it is necessary to perform just sufficient low-pass filtering to prevent the power estimation from being dominated by quantization noise from the 1-bit converter. The bandwidth of the power sense signal, however it may be derived or determined, should be wide enough to cover the frequency band not adequately protected by the partial channel filtering in the analog domain. AGC loop technology (including, but not limited to, conventional AGC loop circuits) is then applied with the aim of keeping the total incident power at the A/D input terminals as high as possible consistent with providing headroom. In various illustrative embodiments of the present invention, the total incident power at the A/D input terminals is between 10dB to 15dB below the full-scale input of the A/D converters, thereby providing for headroom. This headroom is intended to allow for the peak-to-mean ratio of the input signals and interferers, with some allowance for delayed reaction through the AGC loop.

Appropriate decimation and channel filters process the signal such that the wanted channel dominates the final signal. At this point some digital automatic level

control is applied to fit the most significant non-zero bits of the signal in a limited word size for further processing. Such digital automatic level control provides that the changes in gain, which may be determined by the interferer power rather than the signal power, do not influence the final output of the wanted signal, i.e., the signal that is to be demodulated. Both the feedback gain control state and the feedforward digital automatic level control state are known at all times and can be used to determine the absolute level of the wanted signal, which may be needed for soft decision derivation or path loss estimation in the receiver.

Consider, for example, the signal chain analysis for a direct conversion CDMA receiver operating under conditions of a strong single-tone interferer at 900MHz. Table 1, below, provides some illustrative signal levels for both the wanted signal and a 900MHz single-tone interferer.

Signal Level (dBm)	-101.0								
Single Tone Freq (+/- kHz)	900								
Single Tone Level (dBm)	-25.0								
Tx Power (dBm)	24.0								
	ANT	VGA1	LPF1	NULL	LPF2	NULL	LPF3	VGA2	ADC
Power/Voltage Gain (dB)	0.0	16.0	10.0	0.0	10.0	0.0	0.0	12.0	0.0
Cascade Power/Voltage Gain (dB)	0.0	33.5	43.5	43.5	53 5	53.5	53 5	65.5	65 5
Signal Power (dBm/mV)	-101.0	0.189	0.6	0.6	1.9	1.9	1.9	7.5	7.5
Single Tone Power (dBm/mV)	-25.0	1189.9	1189.9	1189.9	945.2	945.2	84.2	335.4	335.4
LNA CrossMod Power (dBm)									
Total Inband Signal+Noise (mV)		0.28	0.87	0.87	2.76	2.76	2.76	10.98	10.98
Total Signal + Noise RMS (mV)		1190.0	1189.9	1189.9	945.2	945.2	84.3	335.5	335.5
Tone Power Ratio (dB)		37.6	61.5	61.5	50.3	50.3	29.7	29.7	29.7
Total Signal + Noise P2P (mV)		3365.8	3365.5	3365.5	2673 3	2673.3	238.4	949.0	949.0
Total Inband Noise (dBm/mV)	-112.5	0.20	0.64	0 64	2 01	2 01	2 01	8.01	8.0
Carrier to Noise Ratio dB)	11 3	-0 85	-0.85	-0.85	-0.85	-0.85	-0.85	-0.85	-0.85

TABLE 1

In the illustrative scenario set forth in Table 1, it can be seen that the output signal is 949 mV pp., and that this signal is dominated by the unwanted single-tone power at 335.4 mV r.m.s., compared to the wanted signal at 7.5 mV. Clearly, considerable digital selectivity (about 40 dB) is needed to bring the unwanted tone to a level below the wanted signal. An assumption in this illustrative scenario is that the input to the A/D will saturate at 1 Vpp., and hence the signal chain is just within the limits for this example, which predicts a 949 mV pp., output to the A/D converters.

However, if the interferer increases by only 1dB to -24dBm, the input to the sigma-delta converter will exceed 1 Vpp., and may clip or become unstable, potentially causing a complete loss of the wanted signal.

Note that the vulnerability described above is not restricted to the 900kHz offset frequency. Due to the use of an elliptic transfer function in the analog filtering, the out-of-band attenuation is slow to increase with frequency as shown in Fig. 2. As can be seen with reference to Fig. 2, offsets in excess of +/- 10MHz are required to guarantee an extra 10dB of attenuation.

Consider an unwanted base station transmitter with 30W ERP, and assuming 0dBi gain (i.e., 0 dB gain with respect to an isotropic radiation pattern) for the mobile receiver, we can calculate the minimum path loss allowable to result in -25dBm unwanted received power. Since 30W is +45dBm, the total path loss is simply 45 + 25 = 70dB. This kind of path loss is usually associated with close-proximity line-of-sight situations, which can be well approximated by the free space path loss equation:

$$A = 20\log_{10} 4\pi d_0/\lambda$$

Taking $\lambda = 3 \times 10^8 / 800 \times 10^6 = 0.375m$, and $d_0 = 100m$, we obtain A = 70.5dB.

This shows that at 800MHz, there is a blocking zone of approximately 100m in radius caused by a 30W transmitter at frequency offsets which do not exceed 10MHz. At PCS frequencies, the blocking zone can be calculated in a similar fashion to be approximately 40m in radius.

In the past it has been a common assumption that the AGC signal should be derived exclusively from the power of the wanted signal and should not be influenced, or captured, by off-channel signals. Consistent with this conventional principle, the RSSI signal used to drive the AGC should be derived after the digital filtering by a baseband processor. This principle is illustrated in Fig. 3.

Referring to Fig. 3, it can be seen that the AGC algorithm is driven by an

estimate of the on-channel signal power derived from $I^2 + Q^2$. Typically, low-pass filtering and a logarithmic function are applied to create the decision variable used to determine the state of the step gain amplifiers **302**. This smoothed logarithmic metric is sometimes referred to as a Received Signal Strength Indicator (RSSI).

However, various performance issues arise from using only the wanted-signal strength in the AGC algorithm of the receiver shown in Fig. 3. More particularly, due to the digital filtering used in the baseband processor, the AGC algorithm is unable to detect out-of-band signals which threaten to exceed an allowable input level of the A/D converters. This vulnerability is likely to manifest itself in an abrupt, and complete, loss of communication once the user (i.e., the receiver) enters a blocking zone, such as those described above. Another potential performance issue, which may arise when using only the wanted signal strength in the AGC algorithm of the receiver, is an unstable condition of the AGC due to in-band energy from distortion products triggering the AGC when in a high-gain state, causing a lower gain setting to be invoked. Once the lower gain setting is invoked, the source of the distortion (e.g., clipping) is removed, causing the high gain state to be invoked again. An oscillation between these two states could therefore occur, thereby effectively disabling the receiver which only uses the wanted-signal strength in its AGC algorithm.

Given the various performance issues which arise from using only the wanted-signal strength in the AGC algorithm of the receiver, various embodiments of the present invention are advantageously designed to avoid capture of the ADC by strong blocking signals. More particularly, various embodiments of the present invention, are designed such that the total signal energy reaching the A/D converters of a receiver does not exceed the maximum allowable input amplitude for stable, linear conversion from analog to digital by those A/D converters.

It is noted that various embodiments of the present invention may use the AGC to implement a scheme wherein the total signal energy reaching the ADC, rather than just the in-band signal power, is used to control gain in the receiver. It is further noted that in such implementations, there is a possibility of a weak wanted-signal being pushed further down into the noise when the AGC, triggered by

interference, sets one or more variable gain amplifiers of the receiver to a low gain state. However, it is believed that given the choice between allowing the A/D input to overload and thereby possibly interrupt communication completely, and pushing a weak signal further down into the noise and thereby reduce signal quality, the latter is preferable.

With respect to various embodiments of the present invention which involve using a digital AGC to avoid large signal overload, the AGC algorithm has access to a wide-band estimate of the signal power incident at the A/D converters. One method of providing this is to take the signal power prior to the digital channel filter and use that to create a supplementary energy estimate. Fig. 4 illustrates the additional signal paths **402a**, **402b**, and **402c**, used to achieve the broadband power estimate in one embodiment of the present invention.

In the illustrative architecture of Fig. 4, the conventional portion of the AGC mechanism is used for the majority of the time. That is, the wanted-signal (which is typically the fully filtered signal) is driving the received signal strength metric which is the basis for the decisions about which of the AGC controlled amplifiers should be in high gain versus low gain states. However, in accordance with the present invention, when the energy from the wide-band signal paths exceeds a certain threshold (typically close to the maximum tolerable signal strength), the AGC algorithm directs the AGC controlled amplifiers to reduce gain accordingly.

Fig. 5 shows a C language code fragment in which an illustrative example of an AGC algorithm in accordance with the present invention is shown. The segment of C language provided in Fig. 5, shows that if the wide-band power estimation exceeds a certain threshold, then the gain setting of the first AGC amplifier is set to low gain mode, irrespective of the narrow-band power estimation.

For the purposes of the illustrative example shown in Fig. 5, it is noted that get_wideband_RSSI_measurement() is a function that returns a wide-band RSSI measurement numerically equivalent to the receiver input level in dBm (where dBm is a measurement of power relative to 1 mW) measured without digital channel filtering, and get_narrowband_RSSI_measurement() is the equivalent function

derived with the use of digital channel filtering. Both of these functions take account of the states of the AGC controlled amplifiers to refer the signal level back to the input of the whole receiver chain.

It is noted that the logic of the AGC processes in accordance with the present invention, may be implemented in hardware, software (or firmware), or a combination of hardware and software. Such software may be executed by conventional microprocessors, microcontrollers, digital signal processors, or by custom designed hardware suitable for executing or otherwise processing said software.

Referring to Fig. 6, a portion of a sigma-delta A/D conversion architecture illustrating access to the wide-band signal used for power estimation is shown. Such sigma-delta A/D conversion architectures provide an opportunity for estimating wide-band power by taking a signal from an intermediate point in the decimation and filtering processing chain. More particularly, Fig. 6 shows one channel of a typical decimation and filtering scheme suitable for use in embodiments of the present invention. Each decimation and filtering stage reduces the bandwidth while increasing the resolution of the signal. Due to noise shaping in the sigma-delta A/D converter, several stages of decimation and filtering are needed to reduce the impact of high frequency quantization noise. Hence a compromise is typically made in choosing a particular point in the decimation chain for power estimation. This trade-off aims to avoid excessive domination by quantization noise, while ensuring sufficient bandwidth for detecting out-of-band interferers.

In various illustrative embodiments described above, two types of power estimation, that is, wide-band and in-band, are used in the AGC algorithms. In an alternative embodiment of the present invention, the complexity of implementation is reduced by only using the wide-band power estimation. In such embodiments the AGC operates only when necessary to prevent overload of the ADC inputs. This does not allow AGC to be used to improve the robustness of the receiver to intermodulation tones, unless those tones were strong enough to trigger an "emergency" reduction in receiver gain to protect the one or more analog-to-digital converters in the receiver. Although this alternative embodiment provides a less complex implementation (because it only uses wide-band power estimation for its

AGC process), it does not generally permit sufficiently early operation of the AGC so as to protect the receiver from intermodulation phenomena.

In the various illustrative descriptions provided herein, it has been shown that receivers that include digital signal processing portions, and which rely to a certain extent on digital selectivity, may be vulnerable to large single-tone interferers at offsets between 900KHz and 10MHz from the wanted frequency. Conventional AGC schemes, which are driven only by in-band signal power, may fail to react to such an unwanted signal even though it threatens to interrupt communications. An improvement of the AGC architecture, in accordance with the present invention, provides a mechanism to detect such signals when they reach a level that threatens to block the receiver and, responsive thereto, reduces receiver gain so as to protect against that eventuality. In one illustrative embodiment, a signal is taken at an appropriate point in the decimation and filtering chain such that it retains wide-band power information.

Various modifications and alterations may be made within the scope of the present invention, including, for illustrative purposes, but not limited to, providing different hysteresis values for different variable gain amplifiers in the receive signal path, or dynamically assigning various wide-band thresholds, narrow-band thresholds, and/or hysteresis values based upon any suitable factors.

It is to be understood that the present invention is not limited to the embodiments described above, but encompasses any and all embodiments within the scope of the subjoined Claims.

What is claimed is:

1. A method of operating a radio receiver having an analog portion coupled to an A/D converter, and the A/D converter coupled to a digital signal processing portion, comprising:

preventing the total signal power reaching the A/D converter from exceeding a maximum allowable input amplitude.

2. The method of Claim 1, wherein preventing the total signal power reaching the A/D converter from exceeding a maximum allowable input amplitude comprises detecting a wide-band signal power greater than a predetermined first threshold, and, responsive thereto, reducing the gain of at least one amplifier coupled to an input terminal of the A/D converter.

3. The method of Claim 2, wherein the A/D converter is a sigma-delta A/D converter.

4. The method of Claim 3, further comprising detecting an in-band signal power greater than a predetermined second threshold, and, responsive thereto, reducing the gain of at least one amplifier coupled to an input terminal of the A/D converter.

5. The method of Claim 1, wherein the radio receiver includes a first variable gain amplifier, and the method further comprises placing the first variable gain

amplifier in a low gain state if a wide-band signal power is greater than a first threshold.

6. The method of Claim 1, wherein the radio receiver includes a first variable gain amplifier, and the method further comprises:

determining that a wide-band signal power is less than a first threshold; and

placing the first variable gain amplifier in a low gain state if a narrow-band signal power is greater than a second threshold.

7. The method of Claim 6, wherein the first variable gain amplifier is placed in a low gain state if the narrow-band power is greater than the second threshold by at least a first hysteresis value.

8. The method of Claim 7, wherein the first variable gain amplifier is placed in a high gain state if the narrow-band power is less than the second threshold by at least a second hysteresis value.

9. The method of Claim 8, wherein the first hysteresis value and the second hysteresis value are the same.

10. A method of preventing saturation of a sigma-delta A/D converter in a radio receiver having digital channel selectivity circuitry, comprising:

obtaining a wide-band power estimation and a narrow-band power estimation;

reducing an amplifier gain of a first one of a plurality of amplifiers if the wide-band power estimation is greater than a first predetermined value; and

if the wide-band power estimation is not greater than the first predetermined value, reducing the gain of at least one of the plurality of amplifiers if the narrow-band power estimation is greater than a second predetermined value.

11. The method of Claim 10, wherein the first predetermined value is selected so as to reduce the occurrence of ADC saturation due to out-of-band signal power.

12. A method of operating a radio receiver having an analog down-conversion portion including a plurality of serially coupled variable gain amplifiers, and a digital portion that performs, at least partially, a frequency selectivity function, the method comprising:

a) setting each of the plurality of variable gain amplifiers to a high gain state;

b) obtaining a wide-band signal power estimate;

c) obtaining a narrow-band signal power estimate;

d) determining if the wide-band signal power estimate is greater than the value of a wide-band threshold;

e) setting a first one of the plurality of variable gain amplifiers to a low gain state if the determination in (d) is affirmative;

f) if the determination in (d) is negative, determining if the narrow-band signal power estimate is greater than the value of a narrow-band threshold; and

g) setting the first one of the plurality of variable gain amplifiers to a low gain state if the narrow-band signal power estimate is greater than the first narrow-band threshold value plus a hysteresis value.

13. The method of Claim 12, further comprising dynamically assigning a value to the wide-band threshold.

14. The method of Claim 13, further comprising dynamically assigning a value to the narrow-band threshold.

15. A radio receiver, comprising:

an analog downconverter including a plurality of serially coupled variable gain amplifiers;

an analog-to-digital converter connected to one of the plurality of variable gain amplifiers; and

a digital baseband processor including selectivity circuitry, and automatic gain control circuitry, the automatic gain control circuitry configured to receive a wide-band signal power estimate, and a narrow-band signal power estimate.

16. The radio receiver of Claim 15, wherein the plurality of variable gain amplifiers are coupled to the automatic gain control circuitry.

17. The radio receiver of Claim 16, wherein the analog-to-digital converter is a sigma-delta analog-to-digital converter.

18. The radio receiver of Claim 15, wherein the automatic gain control circuitry is further configured to receive a wide-band power threshold value and at least one narrow-band threshold value.

19. The radio receiver of Claim 18, wherein the automatic gain control circuitry is further configured to receive at least one hysteresis value.

20. The radio receiver of Claim 16, wherein the selectivity circuitry comprises digital filters.

ABSTRACT OF THE DISCLOSURE

In a radio including analog and digital portions, with at least one A/D converter between the analog and digital portions, and the selectivity of the radio at least partly implemented in the digital domain, an AGC controller sets a first variable gain amplifier (VGA) to low gain upon a determination that a wide-band power estimation exceeds a wide-band threshold. The wide-band threshold is selected to reduce the occurrence of A/D converter saturation. If the wide-band power estimation is less than the wide-band threshold, then for each VGA in the analog portion, a determination is made whether a narrow-band power estimate exceeds a narrow-band threshold, corresponding to that VGA, plus a hysteresis value, in which case that VGA is set to low gain; or whether the narrow-band energy estimate is less than the narrow-band threshold minus a hysteresis value, in which case that VGA is set to high gain.

Figure 1: Receiver chain employing digital selectivity.

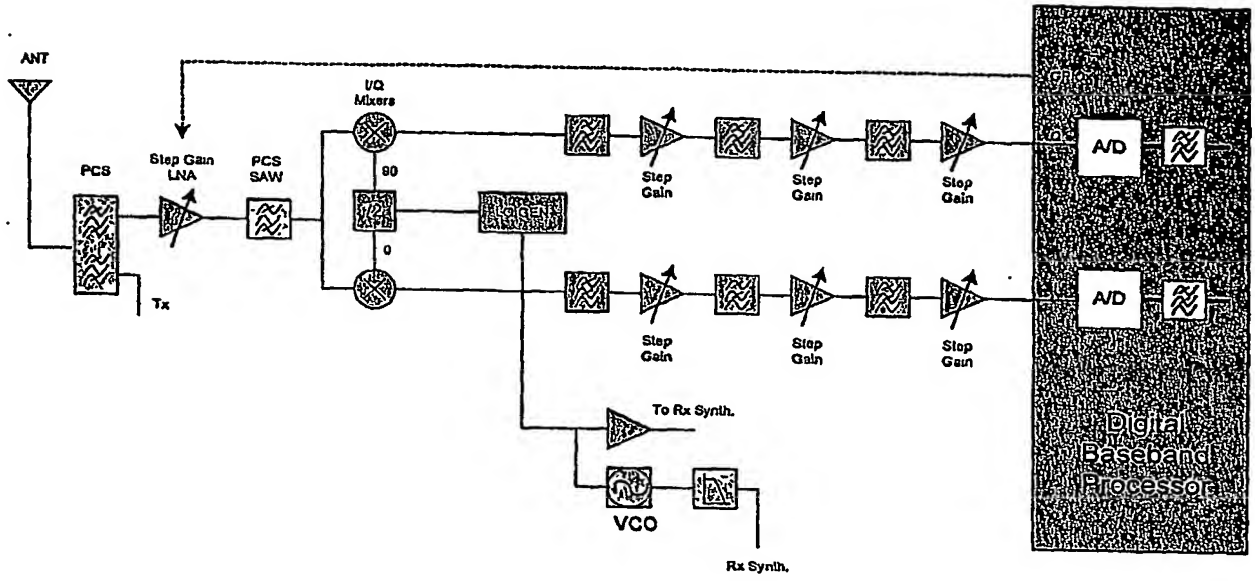


Figure 2: Analog filter transfer function showing wide-band susceptibility

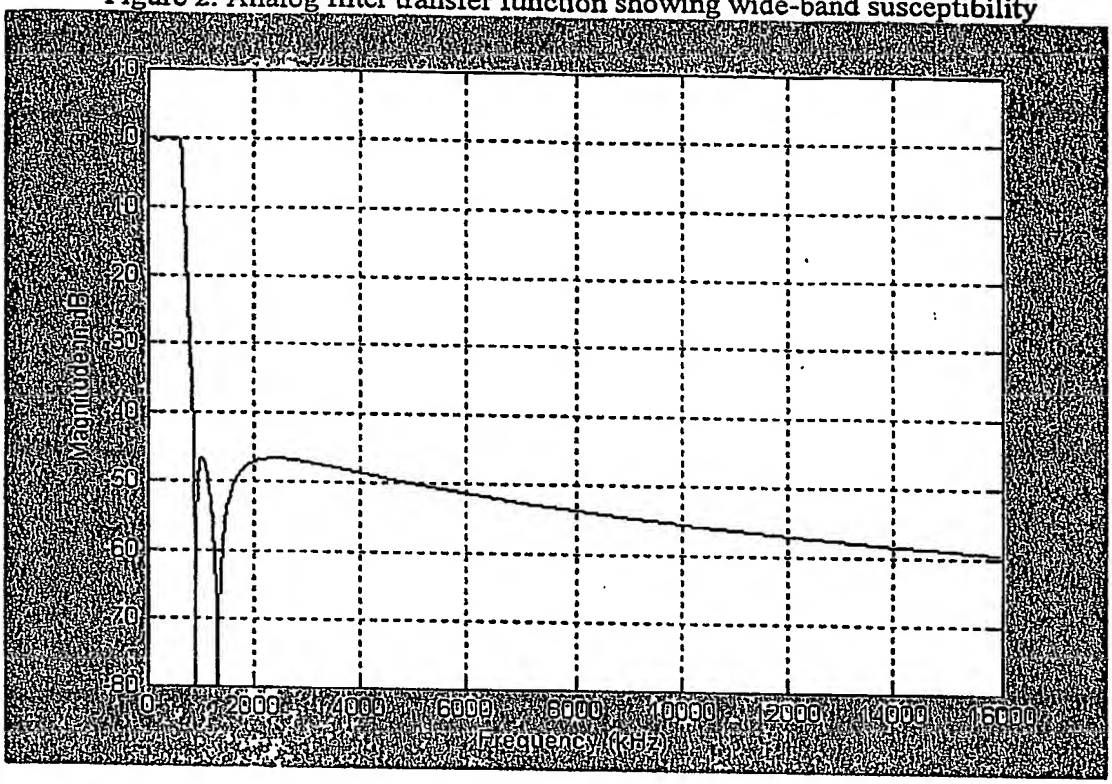
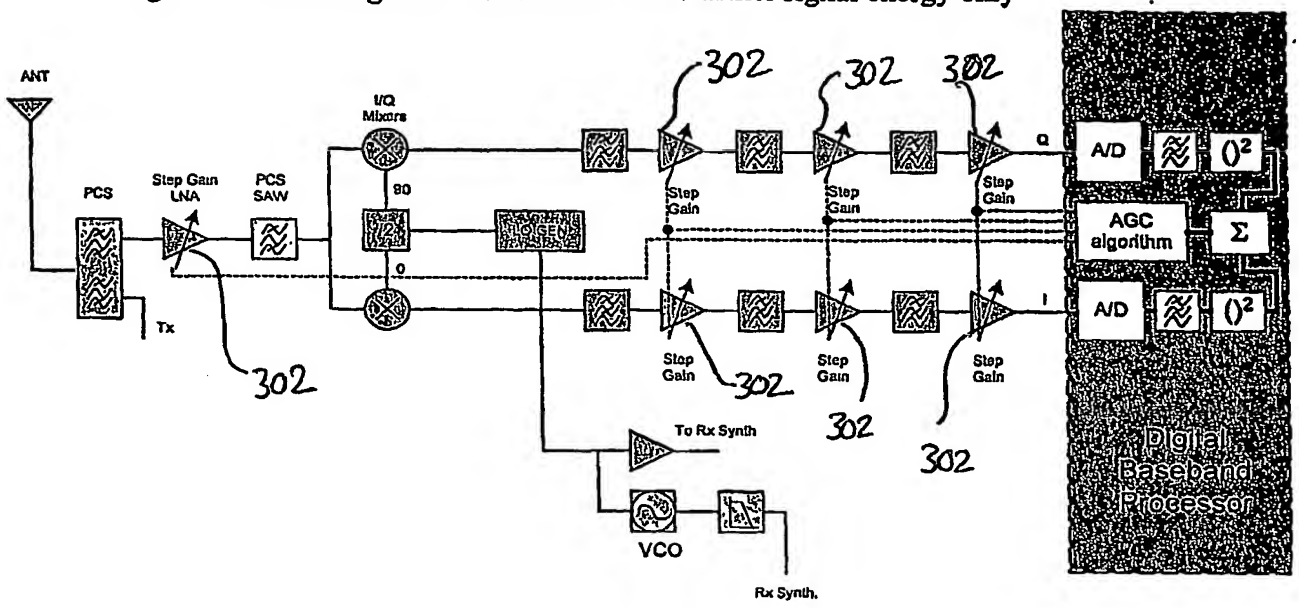


Figure 3: Illustrating AGC derived from on-channel signal energy only



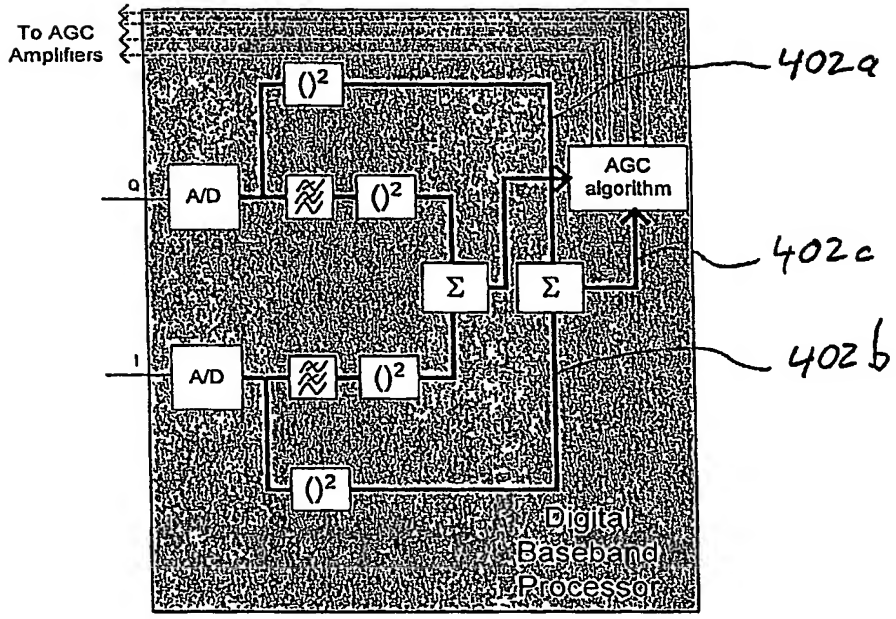

To AGC Amplifiers
()²
402a
AGC algorithm
Q
A/D
()²
Σ
Σ
402c
I
A/D
()²
402b
()²
Digital Baseband Processor

Fig. 4

```
A1=1; A2=1; A3=1; A4=1;          /*  All amplifier gain states set to high gain */
T1=-83;        /* Threshold 1, at -83dBm */
T2=-67;        /* Threshold 2, at -67dBm */
T3=-51;        /* Threshold 3, at -51dBm */
T4=-35;        /* Threshold 4, at -35dBm */
Tw=-28;        /* Wideband overload threshold */
h=3;           /* hysteresis value
do {
        Rw=get_wideband_RSSI_measurement (A1, A2, A3, A4);
        Rn=get_narrowband_RSSI_measurement (A1, A2, A3, A4);
        if (Rw > Tw) then
                A1=0;
        else
        {
                /* normal operation */
                If (Rn>T1 + h) A1=0;
                If (Rn<T1 - h)  A1=1;
                If (Rn>T2 + h) A2=0;
                If (Rn<T2 - h)  A2=1;
                If (Rn>T3 + h) A3=0;
                If (Rn<T3 - h)  A3=1;
                If (Rn>T4 + h) A4=0;
                If (Rn<T4 - h)  A4=1;
        }
        update_AGC_amplifier_states (A1, A2, A3, A4);
        } while (1==1);
```

Fig. 5

Figure 6: Example of access to wideband signal needed for power estimation